REMARKS

Claims 1-31 are currently pending. Claims 32-55 are herein withdrawn. Claims 5, 14, 15, and 17 are herein amended.

The Applicants note with appreciation the Examiner's acknowledgement of the Applicants' information disclosure statements filed in Oct. 2003, Sept. 2005, and Oct. 2005.

In response to the Examiner's restriction requirement, the Applicants affirm election of claims 1-31, and herein withdraw claims 32-55, which may be pursued in one or more divisional applications.

The Examiner has objected to Figure 12 and 13 stating reference characters "1294" and "1394" have both been used to designate "unified model." The Applicant respectfully submits that different reference characters were used for each figure because the unified model shown in each embodiment is not necessarily the same. For instance, in Figure 13, the unified model 1394 includes manufacturing parameters 1302 and electrical parameters 1303. However, in other embodiments, these manufacturing parameters 1302 and electrical parameters 1303 may be external to the unified model 1394. For instance, in Figure 12 the manufacturing parameters and electrical parameters may be included in the input data and controls 1295 (instead of in the unified model 1294). Such an embodiment is discussed, for example, with reference to Figure 25 at paragraph 00125 of the Applicants' originally filed application: "The input data and controls can include generic quantities such as critical dimensions, and manufacturing and electrical parameters of the unified model (2594)." This is why the Applicant's specification, paragraph 00101 discusses "the unified model, together with its associated manufacturing parameters (1302) and electrical parameters (1303)" as noted by the Examiner.

For at least these reasons, the Applicants respectfully request the Examiner to reconsider and withdraw the objection to the Applicants' Figures 12 and 13, as well as the objection to the disclosure at page 25, line 19-20. In addition, the Applicants have amended the specification at paragraphs 00113 and 00114 on page 30 to clarify as suggested by the Examiner.

The Examiner objected to claims 5 and 14. The Applicants have amended as suggested by the Examiner.

The Examiner rejected claims 15-22 under 35 USC § 112, ¶ 2.

With regard to claims 15-18, the Applicants have amended claims 15 and 17 to more distinctly define the claimed invention. With regard to claims 19-22, it is noted that claim 19 further defines the comparing of claim 10 to be carried out using a tolerance (e.g., as opposed to requiring an exact match). The Applicants respectfully submit that one skilled in the art needs no further explanation as how to use a tolerance in the claimed comparing function. There are numerous such uses where comparing generates some result; results satisfying a certain "tolerance" are acceptable, and results not satisfying the tolerance are unacceptable. The Applicants' believe that the present invention should not be limited to any one such use or sub-set of uses, particularly in light of the robust and broad disclosure provided by the Applicants.

For at least these reasons, the Applicants respectfully request the Examiner to reconsider and withdraw the rejection of claims 15-22.

The Examiner rejected claims 1-31 under 35 U.S.C. § 102(e) as being anticipated by U.S. Patent Publication No.2003/0229875 A1 ("Smith").

The Applicants traverse this rejection.

Each of the Applicants' independent claims 1, 10, 28, and 30 defines, in part, a method ... comprising: providing a layout of said target patterned layer; providing a model that includes at least a first parametric representation characterizing at least features of the target patterned layer, and a second parametric representation characterizing at least features of the integrated circuit dependent on one of the plurality of patterned layers other than the target patterned layer; and computing a ... description of a portion of said layout using ... said first parametric representation ... and said second parametric representation. Thus, layout description is computed using two parametric representations, in each of the Applicants' claims.

Smith discloses techniques for using models in integrated circuit fabrication. In more detail, Smith discloses a dummy fill system that minimizes the impact of process variation and subsequent electrical impact "by embedding both a manufacturing process model or simulation and an electrical performance model or simulation inside the dummy fill method." (paragraph # 0111). The dummy fill method is for predicting the manufactured variation in physical and electrical parameters from an IC design. (paragraph # 0132). Note, however, that the models employed are used for a *given* layout, not to *compute* a layout description. In particular, Smith discloses that the "layout may be modified (e.g., through the addition of dummy fill or modification of the design), new layout parameters extracted and evaluation of process variation repeated. This may be repeated until a particular layout yields a desired level of process variation." (paragraph # 0135). Thus, the layout is computed in advance or otherwise provided, and then the models are applied to evaluate process variation. This is further demonstrated by Smith's Figure 15, which describes the steps involved in using calibration models to predict the impact of process variation and subsequent variation in electrical parameters and performance. Significantly, note that a description or set of features relevant to process variation for a number of locations across the chip is extracted or computed from a "new layout or set of layout files as well as desired IC features, geometries and design rule information ... loaded into the system, 30. ... The extracted layout parameters for each spatial location are fed into the model and the resulting process parameters are computed, such as film thickness, dishing, erosion, array and step heights, 33-1. The difference between the target and predicted IC parameters are used to compute the process variation. The predicted process parameters may also be fed into electrical models or simulations to characterize the electrical performance of the IC which when compared with the desired performance allows for the electrical variation to be computed, 33-2. Some of the electrical parameters that may be computed include variation in sheet resistance, resistance, capacitance, interconnect RC delay, voltage drop, drive current loss, dielectric constant or crosstalk noise." (paragraph # 0138; Figure 15).

The Applicants respectfully submit that none of this disclosure (or other disclosure by Smith) discusses or suggests using parametric representations included in a model to compute layout description. Rather, the layout is simply provided or computed in advance by Smith. As such, Smith fails to disclose each and every limitation recited in the Applicants' independent claims 1, 10, 28 and 30 (as well as their respective dependent claims).

Moreover, recall that each of the Applicants' independent claims recites, in part: "... a second parametric representation ... dependent on one of the plurality of patterned layers other than the target patterned layer ... ." Assuming for the purposes of argument that Smith discloses a second parametric representation as perceived by the Examiner, the Applicants further submit that the perceived second parametric representation does not seem to depend on any patterned layer.

For at least these reasons, the Applicants respectfully request the Examiner to reconsider and withdraw this rejection of claims 1-31.

The Examiner rejected claims 1-27 under 35 USC § 102(e) as being anticipated by U.S. Patent No. 6,904,587 B2 ("Tsai").

The Applicants traverse this rejection.

As previously explained, each of the Applicants' independent claims 1 and 10 define a method that includes computing layout description using first and second parametric representations included in a model.

Tsai discloses techniques for incremental lithography mask layout design and verification. In more detail, Tsai performs design rule checking (DRC) by "verifying initial mask layout 330 against a set of manufacturing process rules to identify one or more suitable errors, such as minimum line violations and/or minimum space violations for example, in initial mask layout 330. In addition to or as an alternative to performing DRC, layout verification and analysis tool 352 for one embodiment may simulate the printing of initial mask layout 330 and compare the pattern resulting from the simulated print against the target pattern defined by input layout 310 to identify one or more suitable errors in initial mask layout 330. .... Layout verification and analysis tool 352 for one embodiment may use process model 340 to simulate the printing of initial mask layout 330. (col. 5, lines 27-48). Tsai further states that process model 340 generally corresponds to process model 625. (col. 10, lines 55-57; Figures 3 and 6). Tsai continues by disclosing how the process model 340/625 is generated. In particular, and with reference to Tsai's Figure 6, the process model generator 610 "generates a preliminary process model based on a predetermined set of lithography process parameters 602 to be used to print a target pattern in manufacturing IC 685. Process model calibrator 620 calibrates the preliminary process model based on measurement data 604 to generate a process model 625 that accounts for optical and/or chemical effects not captured by the preliminary process model." (col. 10, lines 46-53; Figure 6). Thus, the preliminary process model is used to generate the process model 625, not to compute any layout description.

As such, the Applicants respectfully submit that Tsai fails to disclose computing layout description using first and second parametric representations included in a model as defined in the Applicants' independent claims 1 and 10 (as well as their respective dependent claims).

Moreover, recall that each of the Applicants' independent claims recites, in part: "... a second parametric representation ... dependent on one of the plurality of patterned layers other than the target patterned layer ... ." Assuming for the purposes of argument that Tsai discloses a second parametric representation as perceived by the Examiner, the Applicants further submit that the perceived second parametric representation does not seem to depend on any patterned layer.

For at least these reasons, the Applicants respectfully request the Examiner to reconsider and withdraw this rejection of claims 1-27.

Also, the Applicants do not concede that either Smith or Tsai has an effective filing date that is prior to the Applicants' date of invention, and the Applicants reserve the right to swear behind Smith and Tsai in accordance with Rule 131.

Based on the above remarks, the Applicants respectfully request the Examiner to reconsider and withdraw the rejection of pending claims 1-31. Favorable action is solicited. The Applicants kindly invite the Examiner to contact the undersigned attorney by telephone, facsimile, or email for quickest resolution, if there are any remaining issues.

Respectfully Submitted,
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